REMARKS

Claims 1 - 22 are pending in this application. Claims 14 - 22 have been withdrawn from consideration and Claims 1 - 13 have been rejected.

By this amendment, dependent Claim 8 has bee canceled and the limitations thereof incorporated into parent Claim 5. In addition, Claims 1, 5, 7, 9, 10 and 13 have been amended.

The Examiner has rejected Claims 1 - 8, 10, 11, and 12 under 35 USC 103(a) as being unpatentable over Fox, et al. (U.S. 4,954,828) in combination with Alcoe and TDK (JP06-181122).

It is the Examiner's position in this rejection that Fox, et al. (Fig. 3, 4) disclose the invention claimed except that "Fox doesn't appear to explicitly disclose that the substrate is a circuit card or that said vias are sloped with respect to said surfaces".

The Examiner goes on to state that Alcoe, however, "teaches that a circuit card is a substrate (Claim 6)" and that "TDK utilizes through hole or vias sloped with surfaces". In regard to the TDK reference, the Examiner further states that "it would have been obvious to one of ordinary skill in the art to form sloped vias in the insulating material of Fox, et al. in order to reduce size as taught by TDK (English Advantage)".

The Fox, et al. patent, relied upon by the Examiner, is directed to a particular packaging arrangement for providing power to widely spaced-apart power contacts on the face of a chip using a compliant interposer. The packaging arrangement of Fox, et al. acts to simultaneously urge the chip into intimate heat-exchange contact with a thermal transfer member or heat sink engaging the backside of the chip and establish power connections directly between the substrate and the chip. The Fox, et al. patent is not concerned with

the CTE thermal mismatch problem between chip and laminate chip carrier addressed by Applicants. As stated by Applicants, the bonding of a chip to chip carrier reduces solder joint stress during thermal cycling but also causes the chip itself to be put under high internal stresses eventually leading to chip cracking, delamination and a device breakdown. To address the problem, Applicants provide a floating interposer which acts as chip carrier and provides stress relief to the electrical interconnections between chip and circuit card by moving on its opposing surfaces relative to the CTE rate of the material with which it is in contact. The floating interposer is a flexible and compliant layer of low modulus material having an array of vias plated with metal arranged to flex and comply, i.e., float, in response to CTE thermal mismatch.

Applicants' Figures 2, 3 and 4 show structural arrangements employed to facilitate this flexing and floating of the compliant interposer. For example, Figure 3 shows the metal-plated vias sloped in a bias arrangement so as to facilitate compliance with the differences in thermal expansion rates between chip and chip carrier. Figure 4 shows another such arrangement of sloped vias that acts to accommodate these differences in thermal expansion rates. Figure 2 shows a way of enhancing the compliance of the interposer material itself.

Accordingly, it can be seen that the Fox, et al. patent is directed to solving a different problem than the problem solved by Applicants. Both the compliant interposer and plated materials in Applicants' invention are designed to float to compensate for thermal mismatch. The Fox, et al. patent fails to teach or suggest anything whatsoever in regard to a floating interposer with sloped vias arranged to compensate for thermal mismatch between chip and substrate.

The Examiner has relied upon TDK for support in regard to Applicants' claimed sloped metal plated vias. However, TDK is directed to a method of manufacturing exciting coils used in inductors and the like and has nothing to do with chip packages. The so-called "sloped vias" of TDK are, in reality, merely a way of continuously connecting the coils from one loop to the next. They are not an array of vias as used in chip packaging. The so-called "via" connection between one loop of the TDK coil and the next does not extend through a layer of flexible or low elastic modulus material.

It is clear that there is no basis whatsoever for combining the TDK reference with the Fox, et al. patent and one skilled in the art would not be motivated to so combine. In this regard, the Examiner states that "it would have been obvious to one of ordinary skill in the art form sloped vias in the insulating material of Fox in order to reduce size as taught by TDK (English Advantage)" (emphasis added). TDK teaches using connected layered loops so as to reduce the size a transformer. The Fox, et al. patent on the other hand, is not directed to transformers or reducing transformer size. Not only is Fox, et al. not directed to transformers or reducing transformer size, Applicants' invention is also not concerned with transformers or reducing transformer size.

Thus, even if Fox, et al. and TDK are combined in some manner, there is no teaching in either reference of sloping vias to facilitate the flexing and floating of a flexible interposer to compensate for thermal mismatch between a chip and substrate. In this regard, the Examiner's rejection of Claims 7 and 8 (paragraph 11) is not understood. The Examiner makes reference here to "dimensions of a sloped via or 'V' shaped via". However, Applicants are not claiming any dimensions in this regard.

Applicants have amended independent Claims 1 and 5 to even more clearly point out what Applicants regard as their invention. Claim 1, for example, now calls for an interposer for connecting a chip directly to a circuit card comprising "a layer of elastic dielectric material having an array of metal plated vias extending from one surface of said dielectric material to the other with each of said metal plated vias terminating in a metal pad and with each of said metal plated vias sloped with respect to said one and said other surface" (emphasis added).

Similarly, Claim 5 now calls for an electronic package comprising a semiconductor chip die and a "flexible layer of dielectric material having an array of metal plated vias extending therethrough in sloped relationship to opposing surfaces thereof" (emphasis added).

None of the references relied upon by the Examiner, either alone or in combination, teach such structure to solve the problem solved by Applicants. In addition, the various dependent claims even further define structure that is neither suggested nor taught by the references relied upon by the Examiner. For example, Claim 7 further defines the metal plated sloped vias as sloped in a V-shaped configuration as shown in Figure 4. In addition, Claim 9, which now depends upon dependent Claim 6, calls for the array of holes between copper plated vias as shown in Figure 2, and Claim 13 calls for the copper plated vias being filled with solder. Again, the references relied upon by the Examiner fail to teach or suggest such structure. It is noted, in this regard, that Brodsky does not teach employing an array of holes as taught by Applicants.

Attached hereto is a marked-up version of the changes made to the Specification and Claims 1, 5, 7, 9, 10 and 13. The attached page is captioned **"VERSIONS WITH MARKINGS TO SHOW CHANGES MADE"**.

In view of Applicants' amendment to the claims and Remarks, Applicants firmly believe that the claims are now in condition for allowance. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the outstanding rejections, allow the claims as now presented and pass the case to issue.

Respectfully submitted,

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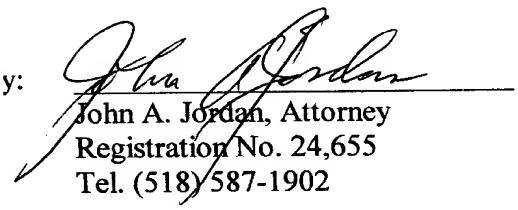
By: 

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"VERSION WITH MARKINGS TO SHOW CHANGES MADE".

With reference to Figure 1, there is shown an interposer arrangement, in partial cross-section, fabricated in accordance with the present invention. Interposer 1 is fabricated from a flexible dielectric layer 3 of low modulus material such as, for example, Rogers 2800 material, Dow 1-4173 material or GE 3281 material. Layer 3 may have an elastic modulus in the range of about 50,000 psi to about 400,000 psi. The thickness of flexible dielectric layer 3 may range between 10 to 15 mils. This may be obtained by laminating several layers of Rogers 2800 material, for example, with heat and pressure to form this thickness. An array of vias 5 are formed in the layer, each approximately 2 mils in diameter. These vias may be fabricated by laser ablation, for example. The array of vias are patterned to match the pattern of connection points on the flip chip die and corresponding connection points on the circuit card chip carrier to which it will be interposed and connected. The vias are then copper plated to form copper walls 6. This may be achieved by first plating all of layer 3 with electroless copper. A plating resist is then applied to the vias and both sides of the layer. A mask is aligned to retain resist in the vias and at sites surrounding the end of the vias so as to form top pads 7 and bottom [pad] pads 9 at the respective ends of the copper walls. Each pad may be approximately 4 mils in diameter. The resist is then exposed and developed and exposed copper on both sides removed after which the resist is stripped off. Further [plaiting] plating may then be carried out. For some applications, the copper plated vias could then be filled with a conductive adhesive composition, if necessary, but the arrangements shown in Figures 5 and 7 use a different approach.

Figure 6 shows another arrangement for attaching interposer 1 to chip die 23. In this arrangement, flexible dielectric layer 3 described in Figure 1 is first laminated to the bottom of chip die 23 before any vias are formed. This may be done by placing the interposer and chip die in a lamination press and subjecting same, depending on materials, to heat (about 180 - 400°C) and pressure (about 250-2000 psi) for at least 1 hour. Then, the interposer material is laser ablated to form vias through to the underside of chip die 23 to expose BLM pads 27. The assembly is then cleaned to remove any contamination on surfaces inside the holes and on the interposer surface and these surfaces are then subjected to electroless copper plating. It can be seen that here, copper deposits not only on via walls at 15 but also at the bottom of the vias at 16 on BLM pads 27. Unwanted copper is then removed using the process described with respect to Figure [5] 1, leaving copper at the bottom and side walls of the holes and at the interposer surface to form pads 9 around the holes. Thereafter, similar to Figure 5, low melt solder balls 29 are attached to pads 9 on the bottom of interposer 1.

1. (Amended) An interposer for connecting a chip die directly to a circuit card comprising a layer of elastic dielectric material having an array of metal plated vias extending from one surface of said dielectric material to the other with each of said metal plated vias terminating in a metal pad and with each of said metal plated vias sloped with respect to said [surfaces] one and said other surface.

5. (Amended) An electronic package comprising:

a semiconductor chip die having an array of conductive pads on one surface thereof;

a flexible layer of dielectric material having an array of metal plated vias extending therethrough in sloped relationship to opposing surfaces thereof with said array corresponding to said array of conductive pads on said chip die and with each of said vias terminating in a metal pad on each of said opposing surfaces with each said metal pad on one of said surfaces electrically connected [by solder] to respective ones of said array of conductive pads on said chip die; and

a circuit card having an array of conductive pads corresponding to said array of metal pads on the other of said surfaces of said flexible layer and connected by solder thereto.

7. (Amended) The electronic package of Claim 5 wherein each of said metal [copper] plated vias of said array of metal plated vias is [flexible layer are] formed by two segments each of which is sloped with respect to an opposing surface of said flexible layer and meet [meeting] internal to said surfaces to form a V-shaped metal [copper] plated via.

9. (Amended) The electronic package of Claim [5] 6 wherein said flexible layer has an array of holes therethrough positioned between said array of copper plated vias.

10. (Amended) The electronic package of Claim [5] 6 wherein each of said copper pads on said one of said surfaces [is] are respectively connected to said array of conductive pads on said chip die by a copper plated connection.

13. (Amended) The electronic package of Claim [5] 6 wherein said copper plated vias are filled with solder.